ABSTRACT OF THE DISCLOSURE

An input/output buffer. An input/output circuit has a transmission terminal coupled to an I/O pad, and a floating N-well region. A P-gate control circuit conveys the second gate control signal to the gate of the first PMOS transistor. A feedback detection device is coupled between the transmission terminal and an N-well control circuit to output a feedback signal according to an input voltage at the I/O pad. The N-well control circuit adjusts the voltage level at the N-well region of the first PMOS transistor according to the feedback signal output from the feedback detection device.